Why CXL[™] technology is requiring **Memory Bandwidth and Capacity Gap**

Increase in SoC core counts requires continued increase in memory bandwidth and capacity, but the gap between such requirements and platform provisioning capability is growing



Memory Bandwidth Requirement

SK Hynix's CXL[™] Memory Proposition **Emerging CXLTM Memory Solution**

- CXL[™] (Compute Express Link) is an open industry standard for high BW, low latency interconnect.



- E3.S (EDSFF form factor)
- CXL[™] on PCle gen 5 x8 lane
- 96GB based on 1a tech DDR5
- DDR5-class BW, Latency within 1 numa hop, Server-Class RAS, best BW/\$

Memory Capacity Requirement

• Using PCIe expansion bus, byte-addressable CXL[™] protocol can improve scaling in memory resources

CXLTM E3.S Benefits

- 82% gains in system memory bandwidth (throughput) per socket
- Up to 2x larger capacity

(At maximum configuration of both 8 native DDR5 and eight x8 lanes CXL[™] Memory cards per socket)

Below is conceptual graphic combining eight 96GB native DDR5 modules with four x8 CXL[™] memory cards



SK hynix CXL[™] memory scales system memory bandwidth and capacity, effectively boosting system performance

Results below demonstrate performance benefits across workloads using SK hynix CXL[™] for added bandwidth and capacity.





Memory configuration for the Benchmark

- Host Memory : 2-channel, 1dimm per channel, 64GB DDR5-4800
- CXL[™] Memory : CXL[™] 2.0 on PCIe Gen5 x8 with 2 sub-ch 96GB DDR5 24Gb 2Rx4 4800
- BW expansion case : With the performance improvement from memory channel increase, execution time can be improved by 19.7% when running a lot of AI/ML and HPC workloads even in the full-channel memory system.
- Capacity expansion case : CXL[™] enables 60.0% larger working set than host only memory system in Redis DB connected with YCSB benchmark without any performance drop. The capacity ratio between host and CXL[™] is 2:1.



Redis+YCSB

OPS(MILLION)